Quartz 5550

3U VPX SOSA aligned 8-channel A/D & D/A board with Xilinx Zynq UltraScale+ RFSoC - Gen 1

Developed in alignment with the SOSA Technical Standard

- High-bandwidth data streaming
- Waveform signal generator
- Communication receiver and transmitter
- Electronic Warfare transponder
- Analog I/O for digital recording and playback
- Sensor interfaces

The Quartz® 5550 is a high-performance, SOSA aligned 3U OpenVPX board based on the Xilinx Zynq UltraScale+ RFSoC. The RFSoC integrates eight RF class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip. The 5550 brings RFSoC performance to 3U VPX with a complete system on a board.

Complementing the RFSoC's on-chip resources are the 5550's sophisticated clocking section for single board and multiboard synchronization, a low-noise front end for RF input and output, up to 16 GBytes of DDR4, a 10 GigE interface, a 40 GigE interface, a gigabit serial optical interface capable of supporting dual 100 GigE connections and general purpose serial and parallel signal paths to the FPGA.

BOARD ARCHITECTURE

The 5550 board design places the RFSoC as the cornerstone of the architecture. All control and data paths are accessible by the RFSoC's programmable logic and processing system. A full suite of Mercury-developed IP and software functions utilize this architecture to provide data capture, timing, and interface solutions for many of the most common application requirements.

SOSA™ Sensor Open Systems Architecture

FEATURES

- Developed in alignment with the SOSA™ Technical Standard
- Incorporates Xilinx® Zynq® UltraScale+™ RFSoC
- 16 GB of DDR4 SDRAM
- On-board GPS receiver
- 10 GigE Interface
- 40 GigE Interface
- Optional VITA 67.3C optical interface for backplane gigabit serial communication
- Dual 100 GigE UDP interface
- Compatible with several VITA standards including: VITA 46, VITA 48, VITA 67.3C, and VITA 65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled
- Unique QuartzXM eXpress Module enables migration to other form factors
- Navigator® BSP for software development
- Navigator® FDK for custom IP development

EXTENDABLE IP DESIGN

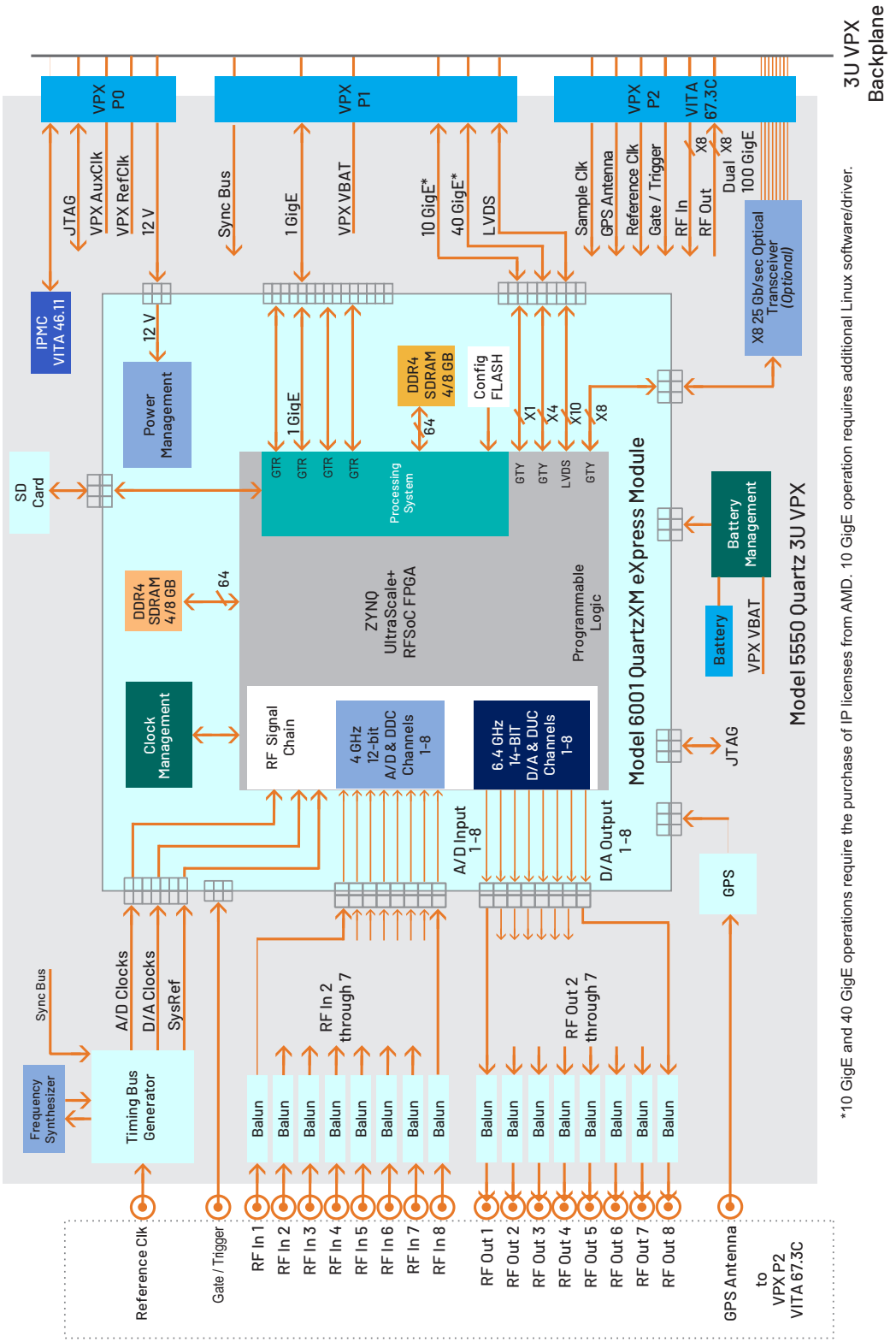
For applications that require specialized functions, users can install their own custom IP for data processing. Mercury's Navigator FPGA Design Kit (FDK) includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado® IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the factory-installed functions or use the Navigator kit to completely replace the Mercury IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 5550's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 5550 either from applications running locally or on the ARMs, or using the Navigator API control and command from remote system computers.

5550 BLOCK DIAGRAM

Click on a block for more information.



*10 GigE and 40 GigE operations require the purchase of IP licenses from AMD. 10 GigE operation requires additional Linux software/driver.

A/D CONVERTER STAGE

The analog interface accepts analog IF or RF inputs on eight coax connectors located within a VITA 67.3C connector. These inputs are transformer-coupled into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 4 GSPS, 12-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x or 8x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor system for signal processing, data capture or for routing to other resources. In addition to the A/D's built-in decimation, an additional stage of IP-based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.

D/A CONVERTER STAGE

The RFSoC's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4 GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x, 4x and 8x. Each D/A output is transformer coupled to a coax connection located within a VITA 67.3C connector.

The D/A gets its sample clock from the A/D clock. Any higher rates to the D/A are achieved only by the use of the PLL in the D/A clock tile.

CLOCKING AND SYNCHRONIZATION

An on-board timing bus generator uses a programmable frequency synthesizer to generate the sample clock and all required timing signals. the on-board sample clock can also be locked to a reference clock received through one of the VITA 67.3C connectors. A multifunction gate/trigger input is also available on one of the VITA 67.3C connectors for external control of data acquisition and playback. For larger systems requiring multiboard synchronization, a multisignal sync bus interface is provided on the VPX P1 connector. These signals include the sample clock and all required complementary timing signals to provide single sample accurate synchronization across multiple boards. The Model 5503 High-Speed Synchronizer and Distribution 3U VPX Board is available as a programmable clocking and sync source for these high channel count Quartz® systems.

MEMORY RESOURCES

The 5550 architecture supports up to 8 GBytes of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, which, along with the Mercury-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. An additional 8 GByte bank of DDR4 SDRAM is available to the Processing System as program memory and storage.

1, 10 AND 40 GIGE INTERFACE

The 5550 includes 1, 10 and 40 GigE interfaces for control and data transfers. These interfaces are independent of the optical 100 GigE interfaces. The 1 GigE interface provides a direct connection to the Processing System. The 10 and 40 GigE interfaces respond to Ethernet ARP requests and are available for custom implementations in SOSA sensor systems.

GPS

A GPS receiver provides time and position information to the FPGA and ARM processors. This information can be used for precise data tagging. The GPS provides a 1 PPS and a reference clock to the FPGA.

EXPANDABLE I/O

The 5550 supports eight 25 Gb/sec full duplex optical lanes to one of the VITA 67.3C connectors. With the built-in 100 GigE UDP interface or installation of a user provided serial protocol, this optical interface enables a high-speed gigabit data streaming path between boards.

INTELLIGENT PLATFORM MANAGEMENT CONTROLLER

The 5550 uses Crossfield Technology LLC's Intelligent Platform Management Controller (IPMC) to provide a fully compliant and flexible management solution for Field Replaceable Units (FRU) that support the VITA 46.11 standard required by HOST and SOSA architectures. The IPMC provides a standardized implementation of FRU management interfaces, control signals, and sensor monitoring. The IPMC provides the Chassis Manager and higher-level System Management Software (SMS) access to FRU information, FRU control signals, and sensor monitoring functions so that they can identify, activate/deactivate, reset, and monitor health of the card and take appropriate system control actions.

The IPMC also provides a low-level path for configuration management and FRU maintenance through both IPMI messages and a Maintenance Port (MP) serial interface. The maintenance port provides a terminal mode command-line interface and supports monitoring, data uploads, and FRU level troubleshooting.

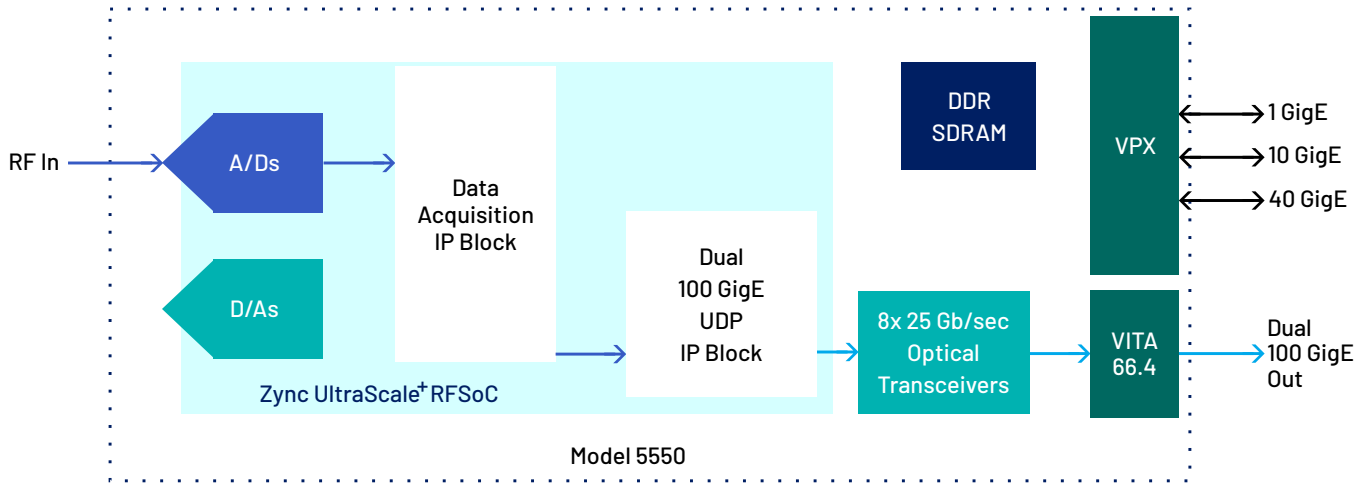
OPTIMIZED IP

Xilinx has created an integrated processing solution in the RFSoC that is unprecedented. The key to unlocking the potential of the RFSoC is efficient operation using optimized IP and application software. Mercury helps streamline the process from development to deployed application by providing a full suite of built-in functions. These address the data flow and basic processing needed for some of the most common applications.

EXAMPLE 1 - HIGH BANDWIDTH DATA STREAMING

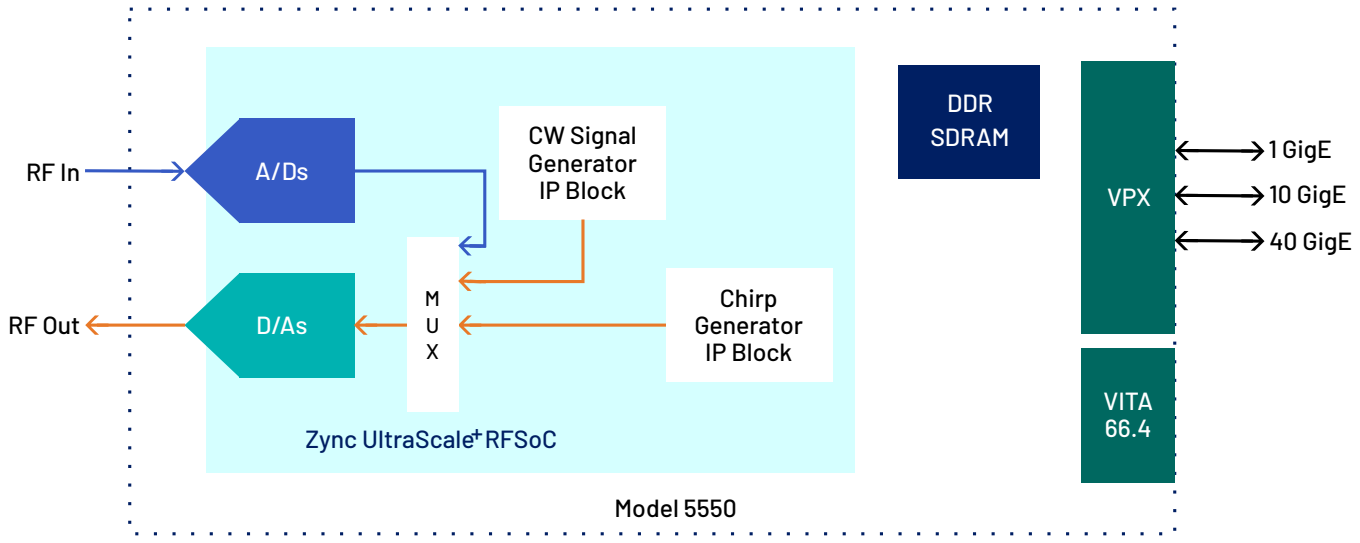
The RFSoC's eight 4 GSPS A/Ds are capable of producing an aggregate data rate of 64 GBytes/sec when all channels are enabled. While capturing this much raw data is not feasible, the A/Ds built-in digital down converters can reduce this data throughput in many applications to a rate reasonable for the data streaming and storage components downstream in the system.

In some applications capturing the raw, full bandwidth data is crucial. The 5550's dual 100 GigE UDP engine provides a high bandwidth path for moving data off of the board. Along with the built-in data acquisition IP, the 5550 can stream two full bandwidth A/D data streams over optical cable to a downstream storage or processing subsystem.



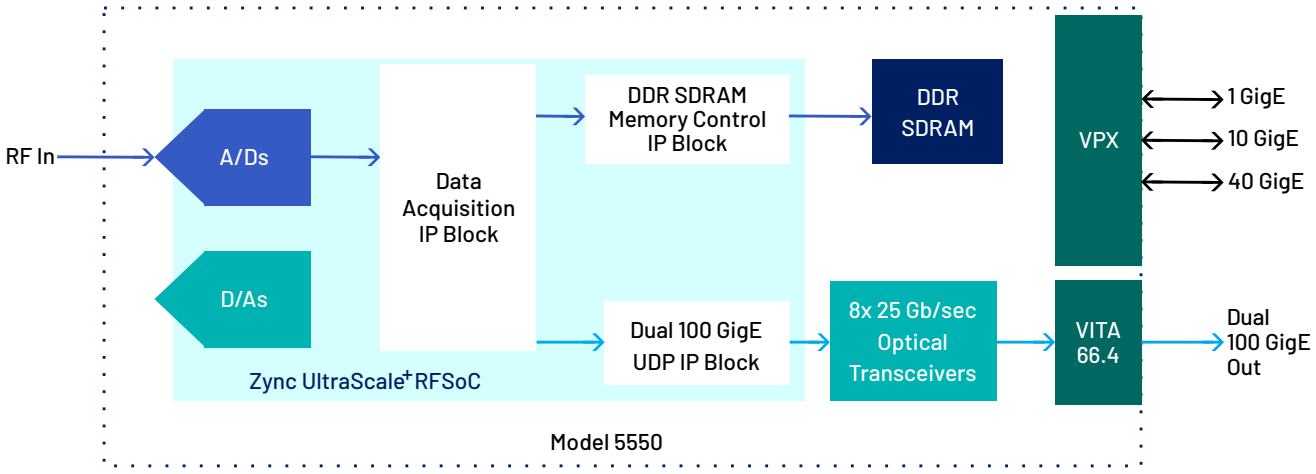
EXAMPLE 2 - WAVEFORM GENERATOR

The 5550's IP supports multiple D/A signal source options. A simple loopback path allows samples received by the A/Ds to be output through the D/As. A CW signal generator produces a sine output with programmable frequency. A chirp generator, ideal for radar applications, outputs sweep signals with programmable frequency, ramp, phase offset, gain offset and length. The generators also include flexible trigger options with both internal and external triggering.



EXAMPLE 3 - MULTIMODE DATA ACQUISITION SYSTEM

In some applications multiple data acquisition modes may need to be operated at the same time. A required dataflow could be full bandwidth streaming of a single A/D channel over 100 GigE to a data recorder while another channel of A/D data is stored as snapshots in the boards DDR4 SDRAM and read by the ARM processor for analysis or transfer over the 1 GigE interface to an external processor. The 5550 provides these modes with built-in IP supporting complex data streaming scenarios without the need for creating custom IP.

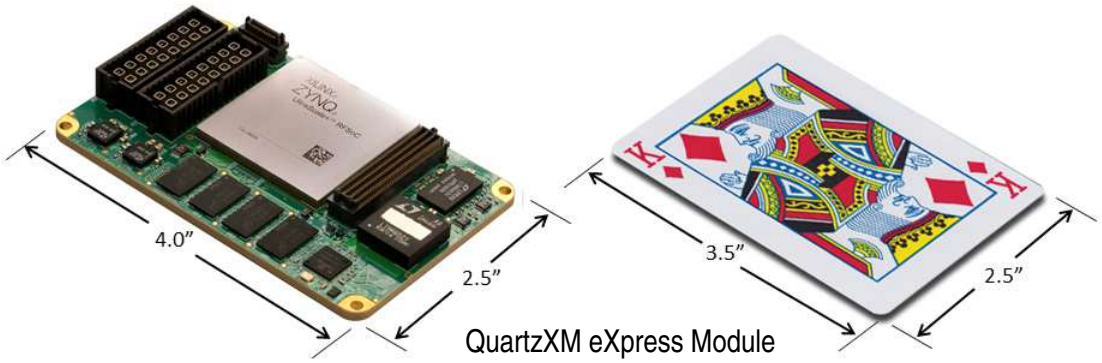


FLEXIBLE MODULAR DESIGN

While the Quartz 5550 follows the form factor of a standard 3U OpenVPX board, the unique modular design of Mercury's 6001 QuartzXM eXpress Module provides the flexibility to deploy this solution in many different situations. The heart of the QuartzXM is a system on module containing all of the key components including the RFSoC FPGA, DDR4 SDRAM, and power and clock management.

In the case of the 5550, the QuartzXM is mounted on a 3U OpenVPX carrier which complements the design with a timing bus generator, analog signal conditioning, a GPS receiver and an 8x 28 Gbps optical transceiver. As a module and carrier board set, the 5550 becomes a complete, ready to deploy 3U OpenVPX solution available for a range of operating environments from commercial to rugged and conduction-cooled.

The 6001 QuartzXM can also be mounted on other carriers available from Mercury to support standard form factors; or for applications that require a non-standard footprint, Mercury supports the module with a design kit for users to engineer and build their own custom carrier. As a complete and tested module, the QuartzXM encapsulates best-in-class electrical and mechanical design, eliminating some of the most challenging aspects of embedded circuit design and allowing the user to focus on the application specific carrier design.



QuartzXM eXpress Module

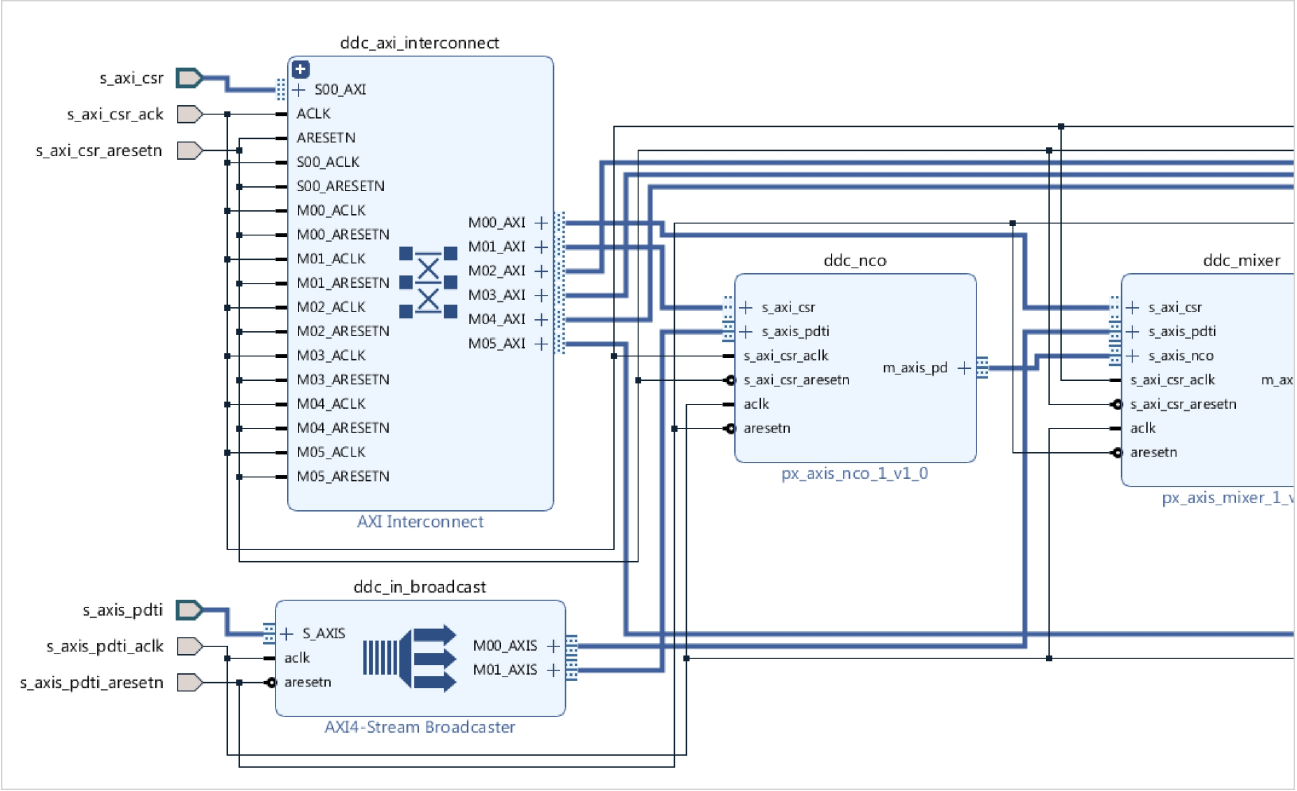
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The Navigator FPGA Design Kit (FDK) for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

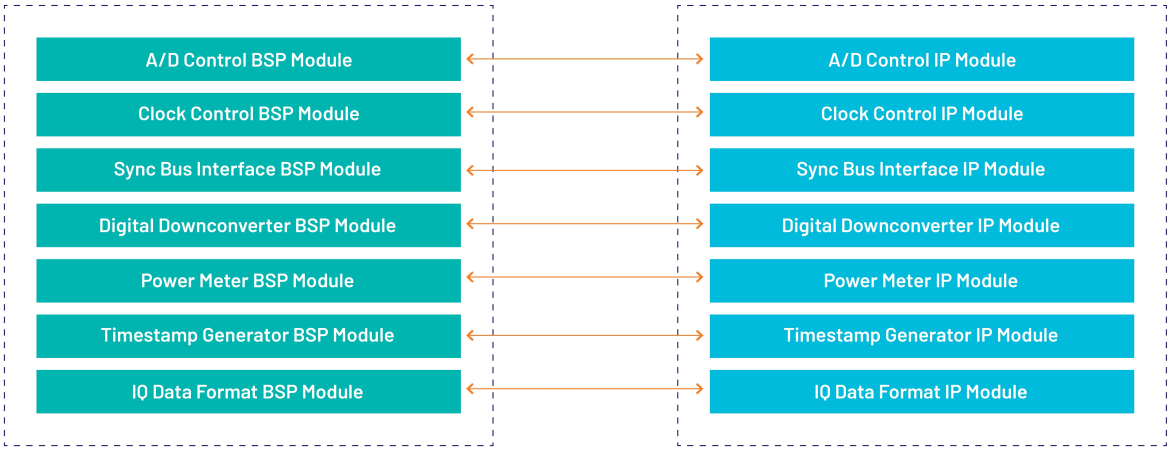
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

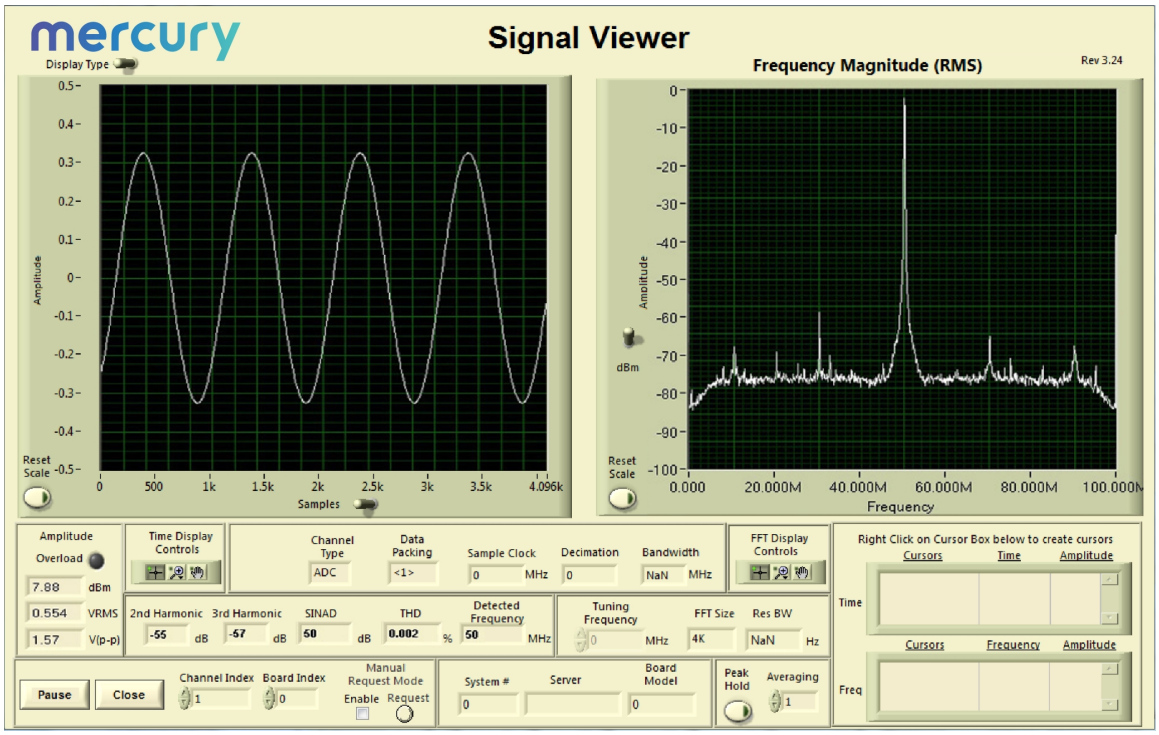
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



SPECIFICATIONS

Field Programmable Gate Array

Type: (standard) Xilinx Zynq UltraScale+ RFSoC XCZU27DR

- Option -028: Xilinx Zynq UltraScale+ RFSoC XCZU28DR

Speed: (standard) -1 speed grade

- Option -002: -2 speed grade

RFSoC RF Signal Chain

Analog Inputs

- Quantity: 8
- Connector: VITA 67.3C
- Input Type: Transformer-coupled
- Transformer Type: Mini-Circuits TCM1-83X+
- Full Scale Input: +10 dBm into 50 ohms (includes matching network)
- 3 dB Passband: 10 MHz to 3700 MHz

A/D Converters

- Quantity: 8
- Sampling Rate: 4.0 GHz
- Resolution: 12 bits

Digital Downconverters

- Quantity: 1 per A/D
- Decimation Range: 1x, 2x, 4x and 8x
- LO Tuning Freq. Resolution: 48 bits, 0 to fs
- Filter: 80% pass band, 89 dB stop-band attenuation

Analog Outputs

- Quantity: 8
- Connector: VITA 67.3C
- Output Type: Transformer-coupled
- Transformer Type: Mini-Circuits TCM1-83X+
- Full Scale Output: +0 dBm into 50 ohms
- 3 dB Passband: 10 MHz to 3700 MHz

D/A Converters

- Quantity: 8
- Sampling Rate: 6.4 GHz
- Resolution: 14 bits

Digital Upconverters

- Quantity: 1 per D/A
- Interpolation Range: 1x, 2x, 4x and 8x
- LO Tuning Freq. Resolution: 48 bits
- Filter: 80% pass band, 89 dB stop-band attenuation

Sample Clock

- Source: On-board programmable clock source or external clock source (from the sync bus only)
- Connector Type: VITA 67.3C (for external source)
- Level: -10 dBm to +10 dBm

Reference Clock

- Source: On-board oscillator, on- board GPS, or external source
- Connector Type: VITA 67.3C (for external source)
- Level: -10 dBm to +24 dBm

Gate/Trigger

- Source: Programmable through software or external source
- Connector Type: VITA 67.3C (for external source)
- Level: TTL

Sync Bus

- Signals: Sample Clock, Reference Clock, Reference Sync, Gate/Trigger
- Location: VPX-P1

RFSoC Processing System

ARM Cortex-A53:

- Quantity: 4
- Speed: 1.5 GHz

ARM Cortex-R5:

- Quantity: 2
- Speed: 600 MHz

Processor I/O:

- Interface: 1 GigE
- Location: VPX-P1

FPGA I/O

Interface: GPIO

- Quantity: 10 Pairs
- Type: LVDS
- Location: VPX-P1

Interface: 10 GigE*

- Location: VPX-P1

*10 GigE and 40 GigE operations require the purchase of IP licenses from AMD. 10 GigE operation requires additional Linux software/driver.

Interface: 40 GigE*

- Location: VPX-P1

*10 GigE and 40 GigE operations require the purchase of IP licenses from AMD. 10 GigE operation requires additional Linux software/driver.

Interface: Optical (Option -108)

- Quantity: 8 full duplex lanes
- Speed: 25 Gb/sec
- Laser: 850 nm
- Location: VPX-P1
- Protocol: Factory-installed dual 100 GigE UDP IP cores provides greater than 24 GB/sec data transfers, other protocols supported with user installed IP

GPS

Source: On-board

Antenna Connector Location: VITA 67.3C

JTAG

Location: VPX-P0

Memory

Processing System:

- Type: DDR4 SDRAM
- Size: (standard) 4 GB
- Option -151: 8 GB
- Speed: 1200 MHz (2400 MHz DDR)

Programmable Logic:

- Type: DDR4 SDRAM
- Size: (standard) 4 GB
- Option -151: 8 GB
- Speed: 1200 MHz (2400 MHz DDR)

FPGA Configuration FLASH:

- Type: QSPI NOR Flash
- Size: 2 x 1 Gbit

Environmental

Option -763: L3 (conduction-cooled)

- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

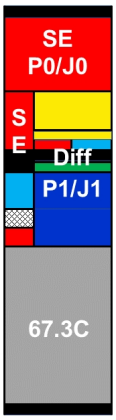
Dimensions: VPX board

- Depth: 170.61 mm (6.717 in)
- Height: 100 mm (3.937 in)
- Weight: Approximately 14 oz (400 grams)

OpenVPX Compatibility

- The 5550 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-1F1U1S1S1U2F1H-14.6.11-12



ORDERING INFORMATION

Model	Description
5550	3U VPX SOSA aligned 8-channel A/D & D/A board with Zynq UltraScale+ RFSoC - Gen 1

Options	Description
-002	-2 FPGA speed grade, -1 standard
-028	XCZU28DR FPGA (XCZU27DR is standard)
-108	VITA 67.3C 8X optical interface
-763	conduction-cooled, Level L3

Contact Mercury for compatible option combinations and complete specifications.

ACCESSORY PRODUCTS

Model	Description
5503	High- Speed System Synchronization and Distribution Amplifier

Option	Description
8256	SOSA Aligned 3U VPX Development Chassis

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