SCFE6931

Configurable, low-latency, 6U OpenVPX™ heterogeneous processing module

AI core board for faster and more efficient processing

- Dual Xilinx Versal® AI Core ACAP processors
- OpenVPX™ compliant for ease of integration
- Supports multiple high reliability cooling options
- Fiber optic interfaces to maximize bandwidth

Mercury's SCFE6931 is a versatile OpenVPX™ heterogeneous processing module designed for high performance and agile system integration. Incorporating Xilinx's Versal® ACAP (Adaptive Compute Acceleration Platform) processors and advanced networking architecture, this advanced module maximizes application performance by combining scalar processing, vector processing and programmable logic into a single 6U design.

Built-in mid-board fiber transceivers enable maximum customization and support high-speed digitization cards. Designed to be delivered in multiple cooling options, the SCFE6931 is ideal for applications that require high-performance operation in harsh environments.

SPECIFICATIONS

Physical

- Single-slot 6U OpenVPX form factor
- OpenVPX interface compliant with ANSI/VITA 65-2010 (R2013)
- Optical mid-board
- Up to 16 Rx/Tx mid-board fiber transceivers per Versal AI Core ACAP

Backplane Interface

- VITA 65 slot profile SLT6-PAY-4F1Q2U2T-10.2.1
- VITA 66.x capable on P3 and P6
- Two Xilinx Versal AI Core VC1902 ACAPs

Memory

- 48 GB of DDR4 SDRAM (24 GB per ACAP)

Other

- Vita 46.11 IPMI controller
- Sensor interface to monitor temperature, voltage
- Power sequencing
- Secure JTAG
- Manufactured in an AS9100D facility

PORTABILITY

Multiple generations of this product family provide the signal processing functionality that enables systems to nimbly respond to emerging threats. Examples include:

- Wideband search using full sample-rate FFTs and threshold detection processing
- Channelizers and multiple independent/coherent digital down/up converter channels with integrated filtering, gain balancing, high-precision receive-time tagging and transmit scheduling, VITA
- 49.x signal data and context packet generation and reception/ depacketizing
- Non-coherent and low-latency coherent EA technique generation
- Communications modem functions
- Instantaneous bandwidths (IBW) in excess of 1 GHz have been implemented and transferred, as well as multiple simultaneous down-converted signal streams of over 100 MHz IBW.

HIGH DATA RATE OPTICAL INTERFACE

Currently implemented at 25 Gbps, the SCFE6931 has integrated mid-board fiber transceivers for connectivity to external system components viva VITA 66.x.

ADVANCED FPGA FUNCTIONALITY

Mercury's processing modules leverage our EchoCore® FPGA IP that allows customers to focus on their application while building on the groundwork to provide basic infrastructure functionality right out of the box. Mercury facilitates the re-use of common IP across FPGAs to optimize time-to-market and reduce development time. Mercury simplifies application integration by providing a standard control plane interface using AXI4-Lite connectivity and uses AXI4-Stream switches for routing data within the FPGA and to external interfaces, such as PCIe. Customers can use their design tool of choice, such as parameterizable Xilinx IPs, HLS or RTL to generate signal processing algorithms. The cores are then instantiated into a reserved user block and compiled into the FPGAs.

ENVIRONMENTAL

VITA - Standard Product
Environmental Qualification Levels

Rugged Level		Conduction-cooled Rugged L3**
Temperature	Operating	-40° C to +71° C (at module edge)
	Storage	-55° C to +125° C
	Max. Rate of Change	10° C/min
Humidity	Operating*	5-95%, non-condensing
	Storage	100% condensing
Altitude	Operating*	0-70,000 ft
	Storage	0-70,000 ft
Vibration	Ran	0.1 g2/Hz; 5-2000 Hz, 1 hr/axis
	Sine	10G peak; 5-2000 Hz, 1 hr/axis
	Shock	z-axis: 50g; x and y-axes: 80g; (11ms, 1/2-sine pulse, 3 positive, 3 negative)
Salt/Fog		10% NaCl
VITA 47		Contact Factory

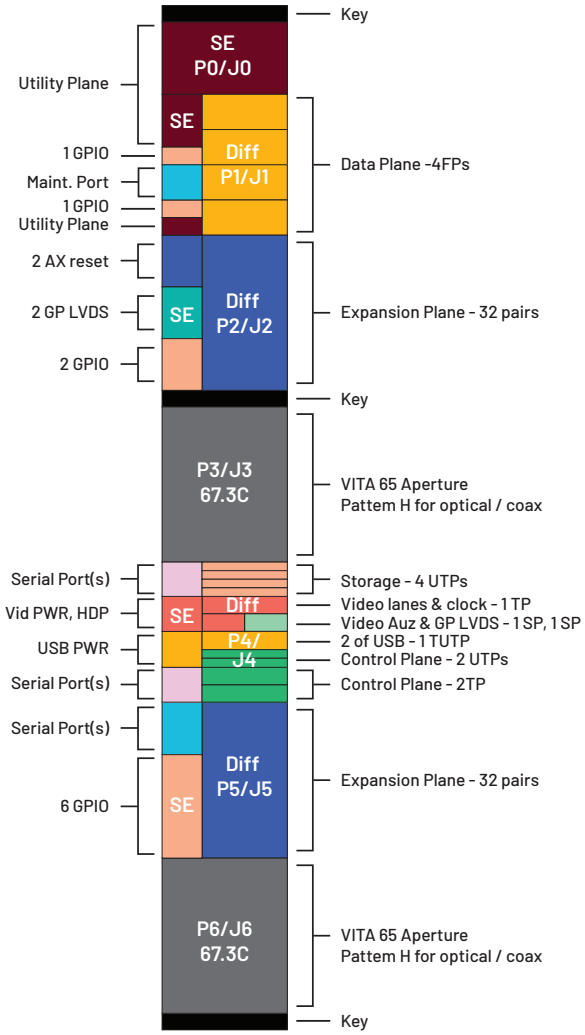
* Customer must maintain required cfm level. Consult factory for the required flow rates.

** Card edge should be maintained below 71° C

Storage Temperature is defined per MIL-STD-810F, Method 502.4, para 4.5.2, where the product under non-operational test is brought to an initial high temperature cycle to remove moisture. Then the unit under non-operational test will be brought to the low storage temperature. The low temperature test is maintained for 2 hours. The product is then brought to the high storage temperature and is maintained for 2 hours. The product is then brought back to ambient temperature. All temperature transitions are at a maximum rate of 10° C/min. One cold/hot cycle constitutes the complete non-operational storage temperature test. This assumes that the board level products are individually packaged in accordance with ASTM-D-3951 approved storage containers. These tests are not performed in Mercury shipping containers, but in an unrestrained condition. Please consult the factory if you would like additional test details.

All products manufactured by Mercury meet elements of the following specifications: MIL-STD-454, MIL-STD-883, MIL-HDBK-217F, and MIL-I-46058 or IPC-CC-830, and various IPC standards. Mercury's inspection system has been certified in accordance with MIL-I-45208A.

SCFE6931 SLOT PROFILE



JUMP-START DEVELOPMENT

Jump-start your development journey with the 8258, Mercury's low-cost 6U VPX development platform ideal for developing applications on the SCFE6931. Providing power and cooling to match the SCFE6931 in a small desktop footprint, the chassis allows access to all required interfaces on the SCFE6931 front panel. The 8258 can be configured with up to eight MPO optical connectors to support the 100 GigE interfaces on the SCFE6931 module.

Further expediting your development efforts, the 8258 comes with Mercury's Navigator Design Suite, which consists of the Navigator FPGA Design Kit (FDK) and Navigator Board Support Package (BSP).

- The Navigator FDK includes a board's FPGA design as a block diagram that can be edited in Xilinx's Vivado IP Integrator. In addition to the IP Integrator block diagrams, all source code and IP core documentation is included. Developers can integrate their own IP along with the factory-installed functions or use the Navigator kit to replace the Mercury IP with their own.
- The Navigator BSP provides a C-callable library for control of a board's hardware and IP.

If deployed, the SCFE6931 board and the code developed with Navigator are portable.

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