Quartz 7053

8-channel A/D & D/A PCIe board with Xilinx Zynq UltraScale+ RFSoC - Gen 3

Quartz PCIe board brings RFSoC performance to PC platforms

- High-bandwidth data streaming
- Waveform signal generator
- Communication receiver and transmitter
- Electronic Warfare transponder
- Analog I/O for digital recording and playback
- Sensor interfaces

The Quartz® 7053 is a high-performance PCIe board based on the Xilinx® Zynq® UltraScale+™ RFSoC. The RFSoC integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip.

The 7053 brings RFSoC performance to PCIe with a complete system on a board. Complementing the RFSoC's on-chip resources are the 7053's sophisticated clocking section for single board and multiboard synchronization, a low-noise front end for RF input and output, up to 16 GBytes of DDR4, a PCIe interface, a GPS receiver, a gigabit serial optical interface capable of supporting user installed protocols and general purpose serial and parallel signal paths to the FPGA.

The 7053 board design places the RFSoC as the cornerstone of the architecture. All control and data paths are accessible by the RFSoC's programmable logic and processing system. A full suite of Mercury-developed IP and software functions utilize this architecture to provide data capture, timing, and interface solutions for many of the most common application requirements.

FEATURES

- Incorporates Xilinx® Zynq® UltraScale+™ RFSoC
- 16 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- LVDS connections to the RFSoC for custom I/O
- Optional front panel dual optical MPO interface for gigabit serial communication
- Unique QuartzXM eXpress Module enables migration to custom form factors
- Navigator® BSP for software development
- Navigator® FDK for custom IP development

EXTENDABLE IP DESIGN

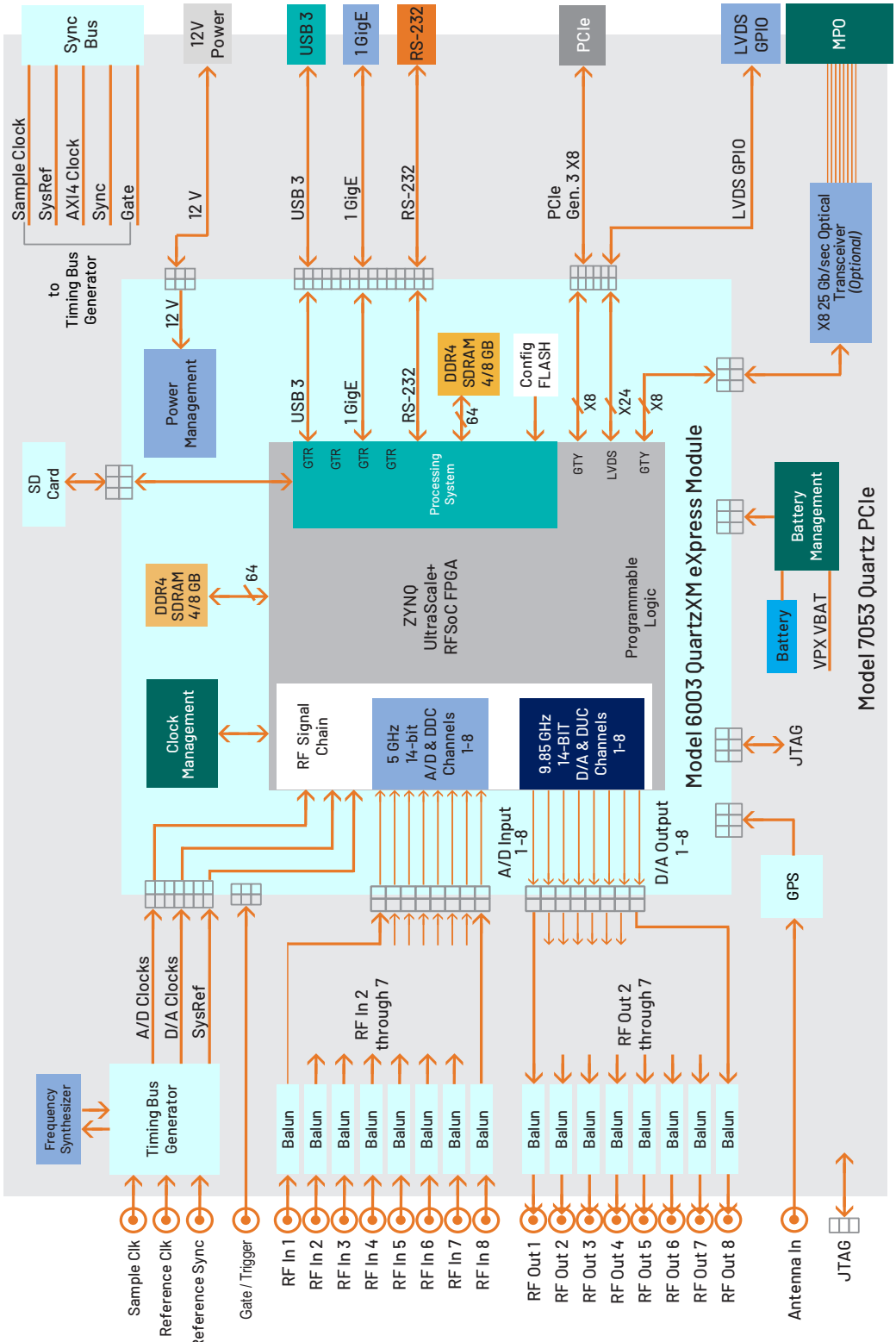
For applications that require specialized functions, users can install their own custom IP for data processing. Mercury's Navigator FPGA Design Kit (FDK) includes the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado® IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the factory-installed functions or use the Navigator kit to completely replace the Mercury IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 7053's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 7053 either from applications running locally or on the ARMs, or using the Navigator API control and command from remote system computers.

7053 BLOCK DIAGRAM

Click on a block for more information.



A/D CONVERTER STAGE

The board's analog interface accepts analog IF or RF inputs on eight front panel MMCX connectors with transformer-coupling into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 5 GSPS, 14-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 3x, 4x 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, or 40x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor system for signal processing, data capture or for routing to other resources.

In addition to the A/D's built-in decimation, an additional stage of IP-based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.

D/A CONVERTER STAGE

The RFSoC's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 9.85 GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, or 40x. Each D/A output is transformer coupled to a coax connection located on the front panel.

CLOCKING AND SYNCHRONIZATION

The Model 7053 front panel includes inputs for sample clock, reference clock, reference sync and gate/trigger. The on-board timing bus generator uses these signals, in addition to a frequency synthesizer, to create the required A/D and D/A clocks and a SysRef for operation of the data converters. The timing bus generator supports an internal clock mode where the sample clock is driven by the programmable frequency synthesizer and no additional clock needs to be provided.

In an alternate mode, the on-board sample clock can be synchronized to a 10 MHz reference clock received through a front panel connector. The Model 7053 can also accept an external sample clock through this front panel connector. This mode bypasses the on-board sample clock. A multifunction gate/trigger input is available on the front panel for external control of data acquisition and playback.

MEMORY RESOURCES

The 7053 architecture supports 8 GB of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, which, along with the Mercury-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications. An 8 GB bank of DDR4 SDRAM is available to the Processing System as program memory and storage.

PCI EXPRESS INTERFACE

The Model 7053 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

GPS

A GPS receiver provides time and position information to the FPGA and ARM processors. This information can be used for precise data tagging. The GPS provides a 1 PPS and a reference clock to the FPGA.

EXPANDABLE I/O

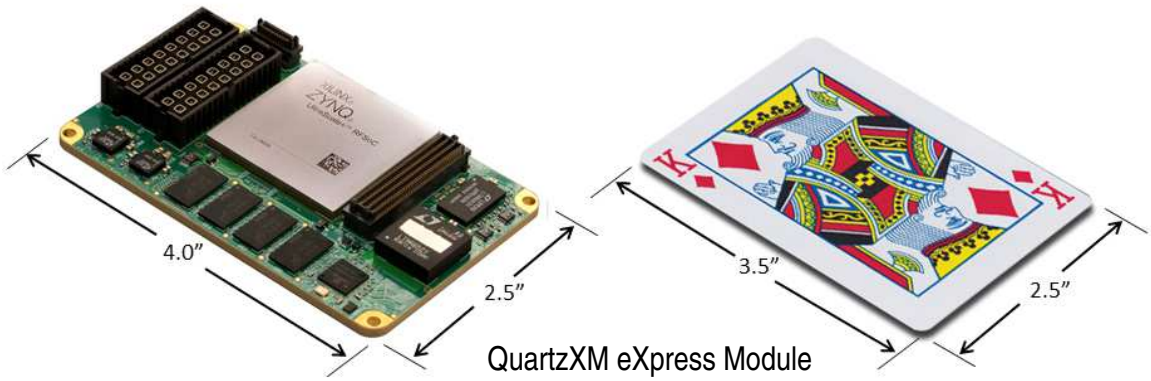
The Model 7053 supports up to eight 25 Gb/sec full duplex optical lanes to a pair of front panel MPO connectors. With the installation of a user-provided serial protocol, the optical interface enables gigabit communications between boards independent of the PCIe interface. Twelve pairs of LVDS connections are provided between the FPGA and a card edge connector for custom I/O. In addition to the front panel analog I/O connectors, the 7053 includes connectors for USB 3, 1 GigE, RS-232, JTAG and a GPS antenna.

FLEXIBLE MODULAR DESIGN

While the Quartz 7053 follows the form factor of a standard PCIe board, the unique modular design of Mercury's Model 6003 QuartzXM eXpress Module provides the flexibility to deploy this solution in many different situations. The heart of the QuartzXM is a system on module containing all of the key components including the RFSoC, DDR4 SDRAM, and power and clock management.

In the case of the 7053, the QuartzXM is mounted on a PCIe carrier which complements the design with a timing bus generator, analog signal conditioning, a GPS receiver and an 8x 25 Gbps optical transceiver. As a module and carrier board set, the 7053 becomes a complete, ready-to-deploy PCIe solution.

The Model 6003 QuartzXM can also be mounted on other carriers available from Mercury to support standard form factors, or for applications that require a non-standard footprint, Mercury supports the module with a design kit for users to engineer and build their own custom carrier. As a complete and tested module, the QuartzXM encapsulates best-in-class electrical and mechanical design, eliminating some of the most challenging aspects of embedded circuit design and allowing the user to focus on the application specific carrier design.



QuartzXM eXpress Module

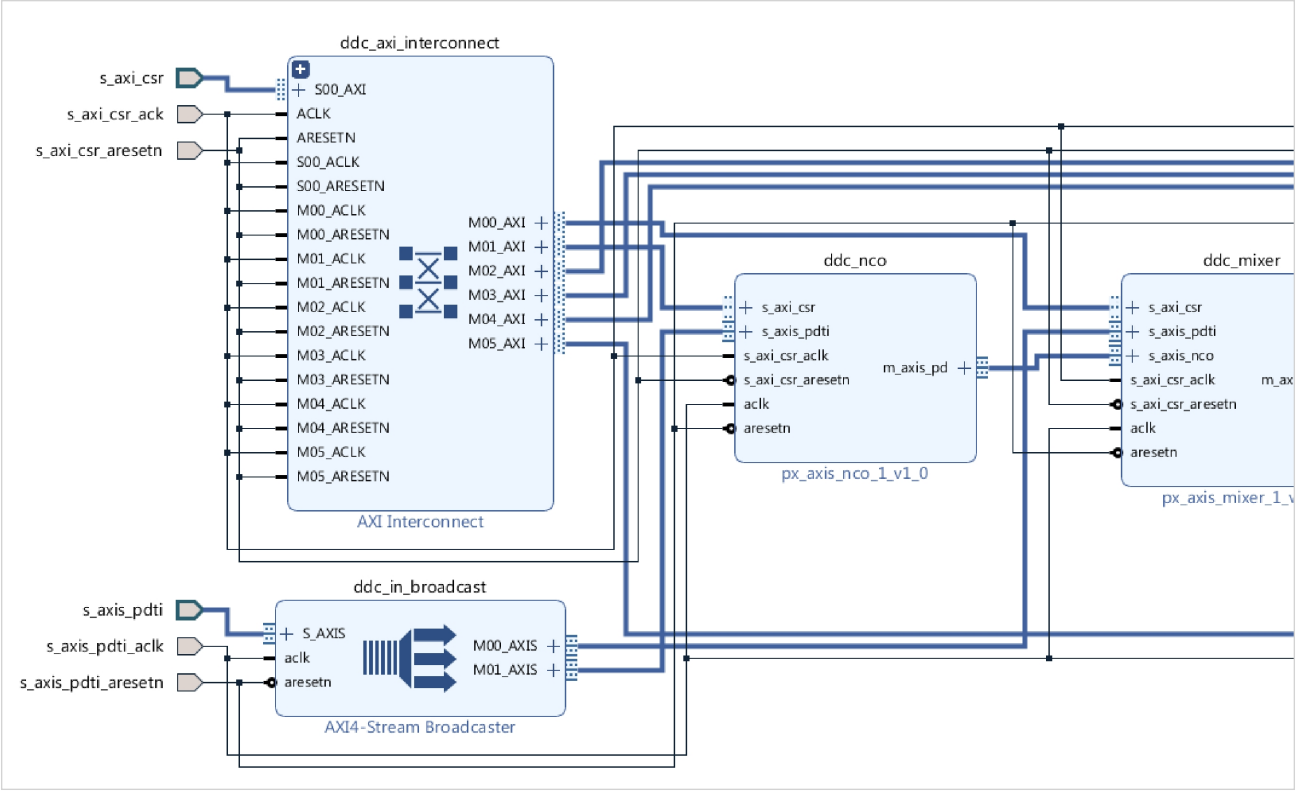
NAVIGATOR DESIGN SUITE

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into the factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

The Navigator FPGA Design Kit (FDK) for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Jade product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Jade design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations.

Navigator FDK includes an IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. multilevel documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.

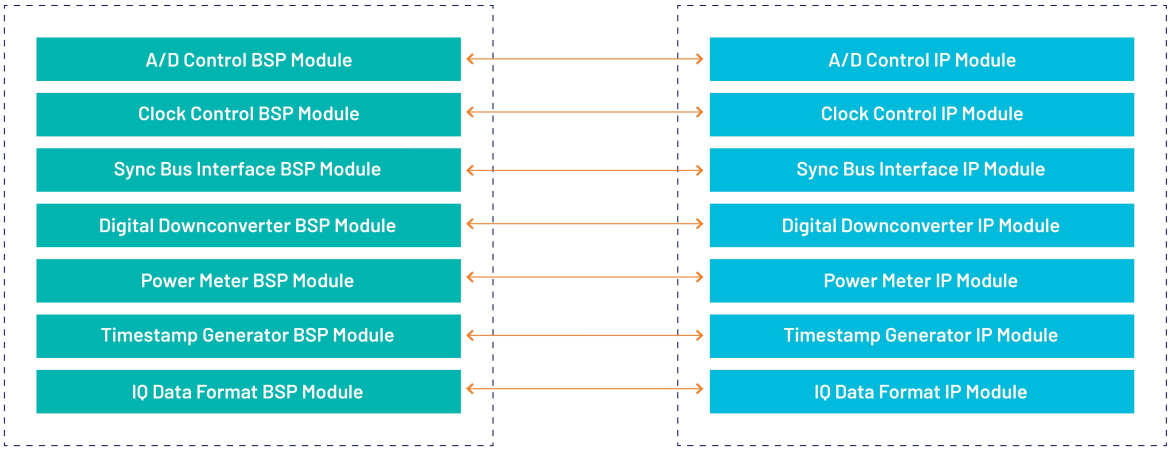
The **Navigator Board Support Package (BSP)** provides software support for Jade boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA. The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



Navigator IP FPGA Design viewed in IP Integrator

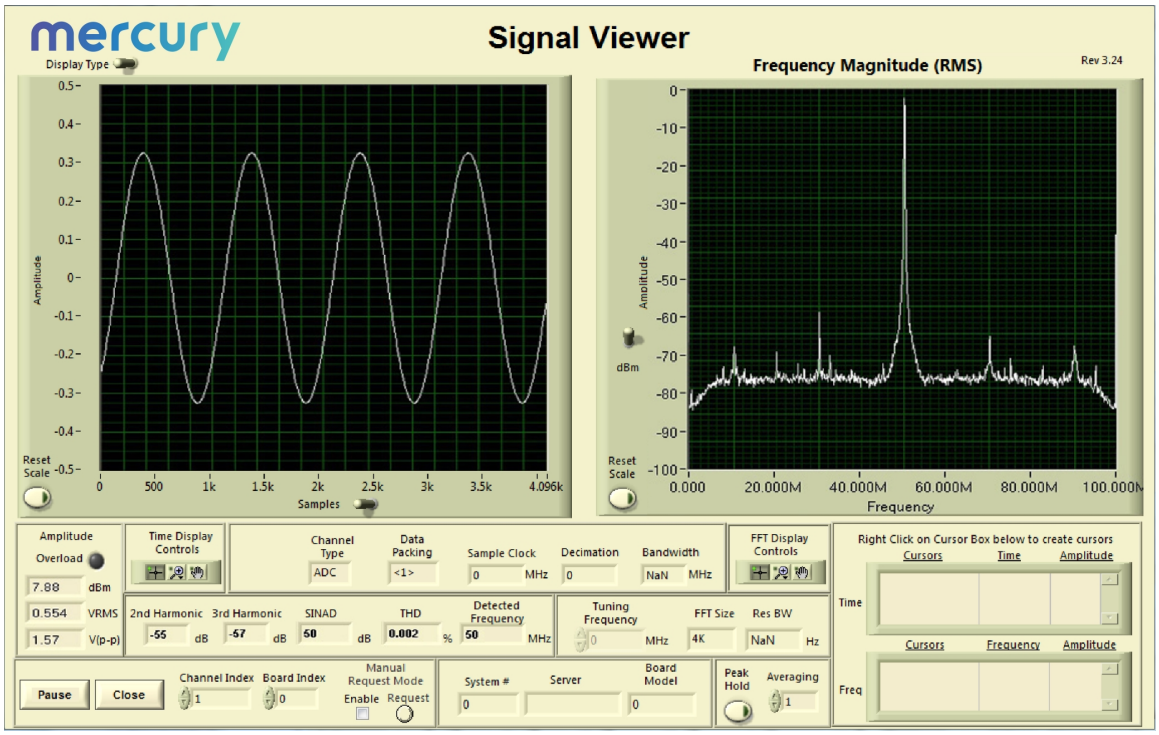
NAVIGATOR BOARD SUPPORT PACKAGE

NAVIGATOR FPGA DESIGN KIT



Because all Jade boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the **Signal Viewer**, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Viewer users can install the Jade board and Navigator BSP and start viewing analog signals immediately.



SPECIFICATIONS

Field Programmable Gate Array

Type: (standard) Xilinx Zynq UltraScale+ RFSoC XCZU47DR

- Option -048: Xilinx Zynq UltraScale+ RFSoC XCZU48DR

Speed: (standard) -1 speed grade

- Option -002: -2 speed grade

RFSoC RF Signal Chain

Analog Inputs

- Quantity: 8
- Connectors: MMCX
- Location: Front panel
- Input Type: Transformer-coupled
- Transformer Type: Mini-Circuits TCM1-83X+
- Full Scale Input: +10 dBm into 50 Ω

A/D Converters

- Quantity: 8
- Sampling Rate: 5.0 GHz
- Resolution: 14 bits

Digital Downconverters

- Quantity: 1 per A/D
- Decimation Range: 1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, and 40x (not all decimations are supported by default IP)
- LO Tuning Freq. Resolution: 48 bits, 0 to f_s
- Filter: 80% passband, 89 dB stop-band attenuation

Analog Outputs

- Quantity: 8
- Connectors: MMCX
- Location: Front panel
- Input Type: Transformer-coupled
- Transformer Type: Mini-Circuits TCM1-83X+
- Full Scale Output: 0 dBm into 50 Ω

D/A Converters

- Quantity: 8
- Sampling Rate: (standard) 8.92 GHz
  - With -2 speed grade (option -002): 9.85 GHz
- Resolution: 14 bits

Digital Upconverters

- Quantity: 1 per D/A
- Interpolation Range: 1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, and 40x (not all interpolations are supported by default IP)
- LO Tuning Freq. Resolution: 48 bits
- Filter: 80% pass band, 89 dB stop-band attenuation

Sample Clock

- Source: On-board programmable clock source or external clock source
- Location: Front panel (for external source)
- Connector Type: MMCX
- Level: -10 dBm to +10 dBm front panel

Reference Clock

- Source: On-board oscillator, on-board GPS, or external source
- Location: Front panel (for external source)
- Connector Type: MMCX
- Level: -10 dBm to +24 dBm

Reference Sync

- Source: Programmable through software or external source
- Location: Front panel (for external source)
- Connector Type: MMCX
- Level: TTL

Gate/Trigger

- Source: Programmable through software or external source
- Location: Front panel (for external source)
- Connector Type: MMCX
- Level: TTL

GPS

- Source: On-board
- Antenna Connector Location: Front panel
- Connector Type: SMA

Sync Bus

- Signals: Sample Clock, Reference Clock, Reference Sync, Gate/Trigger
- Location: Rear edge of card
- Connector Type: Multi-pin, high-speed differential

RFSoC Processing System

ARM Cortex-A53:

- Quantity: 4
- Speed: 1.5 GHz

ARM Cortex-R5:

- Quantity: 2
- Speed: 600 MHz

Custom FPGA I/O

Parallel: 12 pairs of LVDS connections between the FPGA and a top accessible ribbon cable connector

Optical (Option -110): 8X full duplex lanes @ 25 Gb/sec available on front panel MPOs

Memory

Processing System:

- Type: DDR4 SDRAM
- Size: 8 GB
- Speed: 1200 MHz (2400 MHz DDR)

Programmable Logic:

- Type: DDR4 SDRAM
- Size: 8 GB
- Speed: 1200 MHz (2400 MHz DDR)
- FPGA Configuration FLASH: 2x 1 Gb QSPI

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Option -701: L1 (air-cooled)

- Operating Temp: 0° to 50° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Physical

Dimensions:2-slot PCIe

- Width: 1.6 in. (40.6 mm)
- Depth: 8.5 in. (215.9 mm)
- Height: 4.9 in. (124.5 mm)

ORDERING INFORMATION

Model	Description
7053	8-Channel A/D & D/A Zynq UltraScale+ RFSoC Gen 3 Processor - PCIe

Options	Description
-002	-2 FPGA speed grade, -1 standard
-048	XCZU48DR FPGA (XCZU47DR is standard)
-110	MPO 8X optical interface
-701	Air-cooled, Level L1

Contact Mercury for compatible option combinations.

ACCESSORY PRODUCTS

Model	Description
2172	Cable Kit: MMCX to SMA

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810 USA
+1 978.967.1401 tel
+1 866.627.6951 tel
+1 978.256.3599 fax

International Headquarters
Mercury International
Avenue Eugène-Lance, 38
PO Box 584
CH-1212 Grand-Lancy 1
Geneva, Switzerland
+41 22 884 5100 tel

Learn more

Visit: mrcy.com/go/MP7053

For technical details, contact:
mrcy.com/go/CF7053