SCFE6933

Space-qualified, rad-tolerant 6U SpaceVPX heterogeneous processing module

Versal® AI Core processing module for space environments

- Designed for LEO, MEO, GEO, and HEO satellites
- AMD Xilinx Versal AI Core ACAP processor
- SpaceVPX compliant for ease of integration
- Fiber optic interfaces to maximize bandwidth

Mercury's SCFE6933 is a rad-tolerant, high throughput, backend mission data processor ideally suited for demanding sensor applications such as wideband RF and electro-optical/infrared (EO/IR) systems. Incorporating AMD Xilinx's Versal® ACAP (Adaptive Compute Acceleration Platform) processor and advanced networking architecture, this advanced module maximizes application performance by combining scalar processing, vector processing and programmable logic into a single 6U design.

Built-in mid-board fiber transceivers enable maximum customization and support high-speed digitization cards. Specifically designed for space environments, the SCFE6933 is ideal for applications that require high-performance operation in harsh environments.

SPECIFICATIONS

Physical

- Single-slot 6U VPX form factor
- Dimensions:
  233 mm x 160 mm x 25.4 mm
- Compliant with the VITA 78 SpaceVPX standard
- For lab variant: Air-cooled metals
- For flight variant: Conduction-cooled metals
- Up to 12 Rx/Tx mid-board fiber transceivers

System Manager FPGA

- For lab variant: ACT-H3KI-CG624: ProASIC3: A3PE3000-2FG896i
- For flight variant: RTAX-CG624V
- Power: Exclusively from +3.3V_AUX
- Functions:
  - Board management controller
  - Watchdog timer
  - Sensor interface to monitor temperature, voltage
  - Power sequencing

SPECIFICATIONS (CONTINUED)

MGT (Multi-Gigabit Transceiver) Connectivity

- All 44 MGTs are routed to either copper or fiber interfaces.
- 44 MGTs, grouped into 11 Fat Pipes, are routed as described:
  - Copper Data Plane (P1): 4 Fat Pipes (all Hardened Ethernet MAC capable)
  - Copper Expansion Plane (P2): 4 Fat Pipes (all Hardened PCIe capable)

  Note: The Copper threshold MGT line rate is 10 Gb/S.
  - Fiber (P6): 3 Fat Pipes (2 Fat Pipes can utilize Hardened Ethernet MACs from Dataplane). The Fiber threshold MGT line rate is 25 Gb/s.
  - Theoretical Max: 12Rx/Tx @ 25 Gb/s = 300 Gb/s FD (full duplex)

Radiation Tolerance Targets

- Single Event Latch-up (SEL): > 45 MeV/mg/cm2
- Total Ionizing Dose (TID): > 30 krad

Backplane Interface

- Based on VITA 78 slot profile: SLT6-PAY-4F1Q2T-10.2.1
- VITA 66.x capable on P6

Processing

- Xilinx Versal AI Core VC1902 ACAP

Memory

- Configuration Memory (NVM):
  - 8 Gbit Dual QSPI MRAM
  - Capable of supporting multiple images: VC1902 max. image size ~1 Gbit
- Memory for Apps (NVM)
  - 1.333 Tbits of SLC NAND for bulk application storage
  - CONOPS Option: 2 more 1.333 Tbit NANDs available to support TMR
- RAM (Volatile)
  - 4 Banks of stacked DDR4 (ea. 1 Gbit x 64, + ECC [72])
  - Theoretical Max: 2400 MHz x 64 bits x 4 banks ÷2 (FD) = 307.2 Gb/s FD

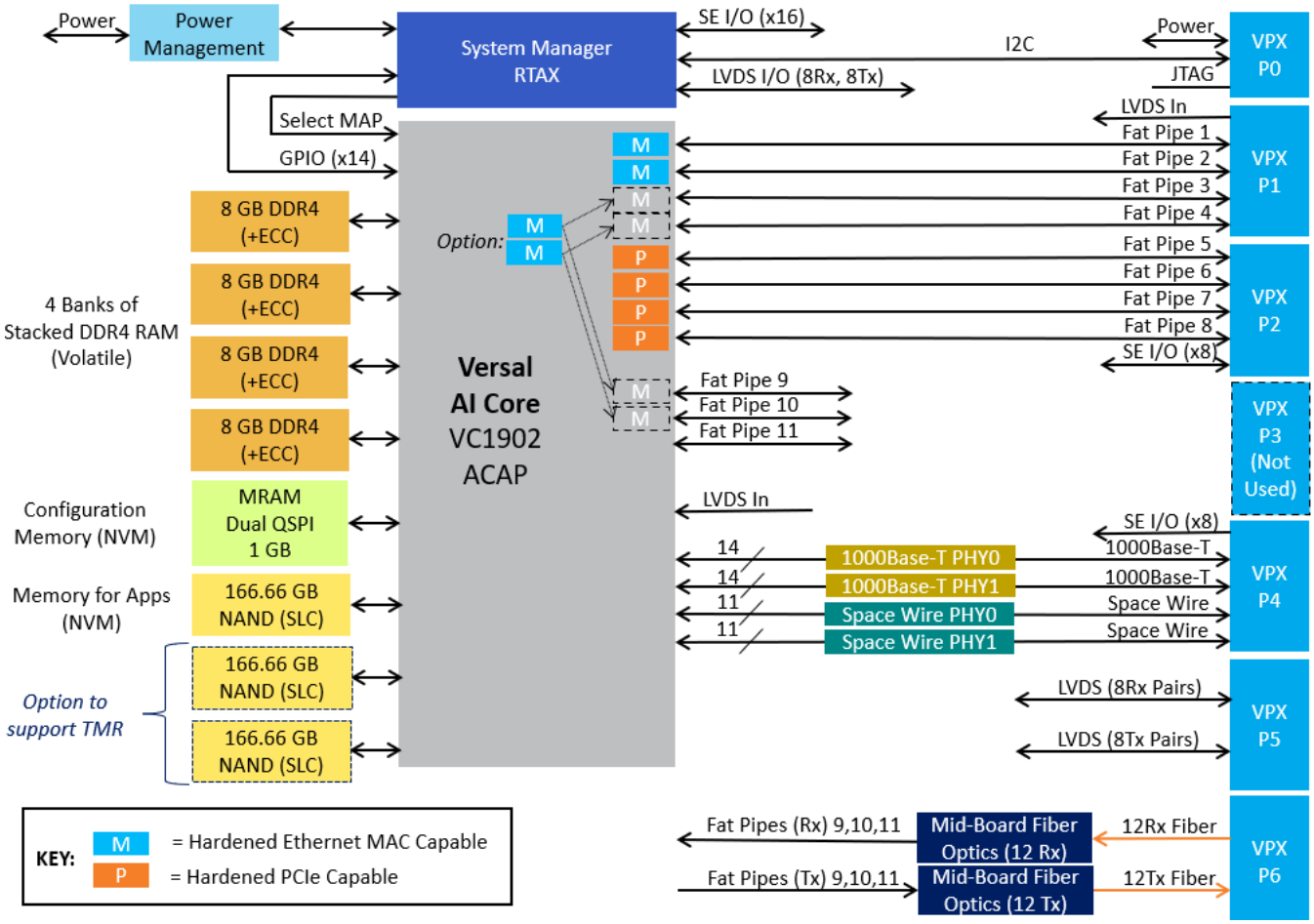
Control & Misc. I/O

- 2 1000 BASE-T ports
- 2 SpaceWire ports
- Utility Plane functions including I2C, JTAG, REF_CLKs, 1PPS
- 5 Rx LVDS Pairs (direct to Versal)
- 8 Tx LVDS Pairs (through RTAX)
- 8 Rx LVDS Pairs (through RTAX)
- 16 SE +3.3V I/O (through RTAX)

Other

- Manufactured in an AS9100D facility

SCFE6933 BLOCK DIAGRAM



THE VERSAL ACAP ADVANTAGE

The heterogenous mix of Versal ACAP resources gives designers the freedom to assign compute power to the processing engine most suitable to the task at hand, and the ability to adaptively reassign resources as required. This flexibility of ACAP delivers as much as ten times the performance over dedicated processor types alone.

Different members of the ACAP family provide different blends of three major processing resources: scalar processors (ARM CPUs), adaptable logic (FPGAs), and vector processors (GPUs and DSPs). These last two resources support AI capabilities such as inference, image processing, pattern recognition and signature detection.

HIGH DATA RATE OPTICAL INTERFACE

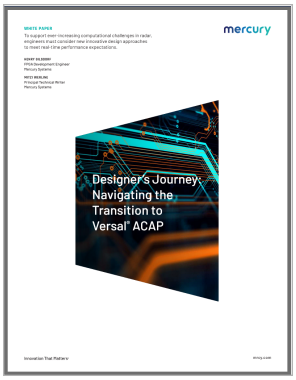
Currently implemented at 25 Gbps, the SCFE6933 has integrated mid-board fiber transceivers for connectivity to external system components via VITA 66.x.

ADVANCED FPGA FUNCTIONALITY

Mercury's processing modules leverage our EchoCore® FPGA IP that allows customers to focus on their application while building on the groundwork to provide basic infrastructure functionality right out of the box. Mercury facilitates the re-use of common IP across FPGAs to optimize time-to-market and reduce development time. Mercury simplifies application integration by providing a standard control plane interface using AXI4-Lite connectivity and uses AXI4-Stream switches for routing data within the FPGA and to external interfaces, such as PCIe. Customers can use their design tool of choice, such as parameterizable Xilinx IPs, HLS or RTL to generate signal processing algorithms. The cores are then instantiated into a reserved user block and compiled into the FPGAs.

DESIGNER'S JOURNEY: NAVIGATING THE TRANSITION TO VERSAL ACAP

This white paper follows a Mercury design engineering team's journey toward ACAP development methodologies. By starting simply, our team was able to better understand the tools and technology behind the ACAP architecture before taking on more complex implementations. Click below to read the white paper.

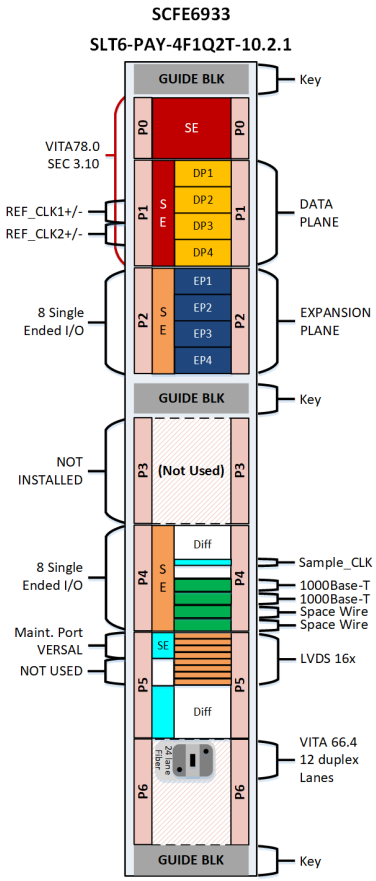


BUILT TO MAXIMIZE VC1902 FOR SPACE APPLICATIONS

Featured Device: VC1902	Supporting Module: SCFE6933
GTY Transceivers: 44	All 44 MGTs routed to backplane over either copper or fiber interfaces
DDR Memory Controllers: 4	4 Banks of stacked DDR4 (ea. 1 Gbit x 64, + ECC [72])
Intelligent Engines: 400 AI Engines 1,968 DSP Engines	Power/Thermal solution designed for 70% utilization of all VC1902 resources with high toggle/clock rates at maximum junction temperature, including 100% GTY and DDR4 utilization.
Adaptable Engines: 899,840 LUTs	
Scalar Engines: Dual-core Arm Cortex-A72 Dual-core Arm Cortex-R5F	
Memory: 482 Mb total	

SCFE6933 SLOT PROFILE

VITA 78 slot profile: SLT6-PAY-4F1Q2T-10.2.1



ORDERING INFORMATION

Model	Description
SCFE6933	Space-qualified Versal® AI Core FPGA processing board - 6U VPX

RELATED PRODUCTS

Model	Description
SCFE6931	Dual Versal® AI Core FPGA processing board - 6U VPX (not space-qualified)

SCFE6931

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Learn more

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