DATASHEET

Secure Solid State Drives (SSD)
TRRUST-Stor® BGA

MBAxxxAM6S-000Ixx-aa

- **Engineered to CSfC, FIPS 140-2, and Common Criteria (CC) requirements (Planned)**
- **SATA and NVMe models**
- **Supports all popular military sanitized protocols plus non-thermal self-destruct**
- **AES-256 XTS encryption with user fillable keys**

ADVANCED*

Mercury Systems TRRUST-Stor BGA SSD modules allow integration of high capacity secure storage directly onto printed circuit boards. Directly attaching the storage to the PCB eliminates the cost and reliability issues associated with cumbersome high-speed cabling. It also removes the potential for tampering by hot-swapping the data cable or probing plaintext data running from the host to the SSD. Featuring all the security capabilities of the popular ASURRE-Stor SSD, the Mercury TRRUST-Stor BGA SSD product line incorporates Mercury's Sixth Generation Armor® NAND Processor and 3D TLC NAND running in SLC mode. The TRRUST-Stor BGA is available with a 6 Gb/s SATA interface or a blazingly fast, 4-lane, NVMe interface.

Features

- Designed, manufactured in a secure DMEA-accredited facility
- Size: 32mm x 22mm x 3.5mm (BGA) (Preliminary)
- Mercury proprietary Armor 6 NAND processor
- 3D TLC NAND running in SLC mode
- AES-256 XTS encryption
- Customer controllable boot partition for authentication
- NMVe and SATA models
- Host accessible capacity: 80, 160 GB[1]
- Total Bytes Written: 1.6 PB (160 GB model)
- FIPS 140-2 and CSfC certified models F and C suffix (planned)
  - Compliant to the NIAP EE and AA protection profiles
  - Multiple key management modes including user defined boot image
  - User and Crypto Officer Roles
- AES Key-Flipper technology eliminates key burn-in
- Fast Clear: Less than 10 seconds
- Self-Destruct capability.
- Supports all popular military sanitization protocols
- DS-101 support for SKL and CYZ-10 compatibility
- Sequential performance
  - 1000 MB/s (4 Lane NVMe, 160 GB model)
  - 540 MB/s (SATA, 160 GB model)
- Ultra-strong LDPC Hard/Soft Error Correction
- UBER (Uncorrectable Bit Error Rate): 10^{-18}
- Leaded BGA balls
- Hot Swap capable
- MTBF: 2 million hours @ 25 °C, Telcordia
- Shock/Vibration: Dependent on mounted environment
- Operating Temperature: -40 °C to +85 °C[3]
- Storage Temperature: -55 °C to +105 °C[3]
- Humidity: 95%, non-condensing
- Altitude: 80,000 feet
- Weight: 8 grams
- Voltages: 3.3V, 1.8V, 1.2V, 0.72V
- Power: 5W (TBD)

Optional Features

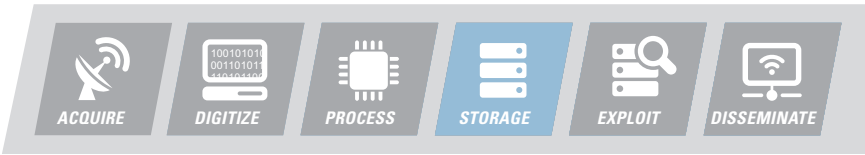
- Extended temperature and burn-in screening
- Capacity de-stroking
- Custom Identification text for re-branding

NOTES:

1. *One Gigabyte (GB) = 1,000,000,000 bytes. 100 MB/s = 100,000,000 bytes per second.*
2. *Performance values based on 128 KiB sequential transfers and largest capacity model.*
3. *Data retention can diminish with extended storage at temperatures above 70 °C. Operation at 85 °C requires maintaining BGA surface at 85 °C or less.*

** This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.*

Mercury Systems is a leading commercial provider of secure sensor and safety-critical processing subsystems. Optimized for customer and mission success, Mercury's solutions power a wide variety of critical defense and intelligence programs.



Ball Descriptions

Ball No.	Ball Name	I/O	Description
A5	UP_KEYFILL_232TX	OUT	Isolated Key-Fill port TX output. This is an LVTTL[1] RS-232 Transmit line from this module to the host system.
A7	DN_ KEYFILL_232RX	IN	Isolated Key-Fill Daisy Chain RX input. This is the LVTTL RS-232 Receive line from a downstream module to this module. This signal is used when multiple SSD modules are daisy chained together.
A26	WRITE_ PROTECT_N	IN	Write protection. When this input is low, host write commands are inhibited.
A28	MOD_ACTIVE	OUT	This is an output notifying the host that the module successfully booted and is ready for normal operation.
B5	UP_KEYFILL_232RX	IN	Isolated Key-Fill port RX input. This is an LVTTL RS-232 receive line from the host to this module. The host uses this signal to send the AES 256 encryption key to this module. The module may output the key on the DN_KEYFILL_232TX to fill the key of a downstream daisy chained module.
B7	DN_KEYFILL_232TX	OUT	Isolated Key-Fill Daisy Chain TX output. This is the LVTTL RS-232 Transmit line from this module to the downstream module. This signal is used when multiple SSD modules are daisy chained together. The data transmitted from this port is data received by the UP_KEYFILL_232_ RX signal of the down stream module.
B25	PS_LOW	IN	This is a high true input that indicates that the voltage PS_PWR is too low for safe operation. PS_PWR is the name the module uses for the voltage rail that is used to derive the supplies that power the module. The module uses the PS_LOW signal to trigger a deterministic shutdown process. When the module detects a high level on PS_LOW, it immediately saves all critical volatile data in non-volatile memory and transitions to an idle state. The host must continue to maintain all voltages suppled to the module for 20 ms after asserting the PS_ LOW signal. The module restarts normal operation when PS_LOW returns to a low level for at least 100 ms.
B27	LINK_SPEED_LED	OUT	Interface connection speed indicator. This signal indicates the link speed that the module negotiated with the host system. For SATA models, this signal is high when the link speed is 3 Gb/s or 1.5Gb/s and is low for a 6 Gb/s link. For NVMe models, this signal is high for link speeds of 2.5 Gb/s and 5 Gb/s and low for a link speed of 8 Gb/s.
C28	ERASE_TRIGGER	IN	This input, when high for 10 ms, can trigger a Secure Erase operation that erases the AES key value and/or the NAND media. This input contains a weak internal pulldown.
C30	FACTORY_LED	OUT	Reserved for use by Mercury systems
D1	NVMe0_SATA_ RX_P	IN	For SATA models, this is the positive high speed SATA receive signal from the host to the module. For NVMe models, this signal is the positive receive signal for Lane 0 from the host to the module.
D2	NVMe0_SATA_ RX_M	IN	For SATA models, this is the negative high speed SATA receive signal from the host to the module. For NVMe models, this signal is the negative receive signal for Lane 0 from the host to the module.
D29	DESTRUCT	IN	When the module is configured to allow a Destruct operation, this signal will trigger a non-reversible self-destruct operation when the module detects a transition of this pin from a low level then to a high level and remaining at a high level for a minimum of 10 ms. To avoid accidental destruct operations, the module ignores self-destruct requests when the signal is detected high at power on time. The signal must be sampled low, once, after the module boots to arm the self-destruct trigger and enable monitoring for a destruct trigger.
D30	SHUT_DWN_N	IN	This is a low true input to the module that allows a host system to request that the SSD module perform an immediate backup operation and then enter a low power shutdown state.
D31	ACTIVITY	OUT	This is a high true output that indicates the module is actively executing a host operation. This signal is intended to drive an external FET to illuminate an LED. This signal cannot directly drive an LED.
E29	DUALPORTEN_N	IN	This is the NVMe dual port enable signal. The input contains a weak internal pullup. Dual port operation is planned in a future firmware release. Leave this pin floating.
E30	AUTH	IN/ OUT	This ia a bi-directional signal that is used by the module to communicate with an external Atmel ATSH204A crypto authentication device.
F1	NVMe0_SATA_ TX_P	OUT	For SATA models, this is the positive high speed SATA transmit signal from the module to the host. For NVMe models, this signal is the positive transmit signal for Lane 0 from the module to the host.
F2	NVMe0_SATA_ TX_M	OUT	For SATA models, this is the negative high speed SATA transmit signal from the module to the host. For NVMe models, this signal is the negative transmit signal for Lane 0 from the module to the host.
F31	BKUP_MEASURE	IN	Voltage input that allows the module to measure the voltage of the external backup power supply. The external backup power supply voltage must be scaled so that a 5V rail is presented as 1.2V to the module.
G29	FPGA_TMS	IN	Reserved for future use. This pin must be left open.
H1	NVMe1_RX_M	IN	For NVMe models, this signal is the Lane 1 negative receive signal from the host to the module.
H2	NVMe1_RX_P	IN	For NVMe models, this signal is the Lane 1 positive receive signal from the host to the module.
H30	FPGA_TCK	IN	Reserved for future use. This pin must be left open.
J29	FPGA_TDI	IN	Reserved for future use. This pin must be left open.
J31	KEY_LED	OUT	This signal goes high to indicate to a user that the module is waiting for entry of the encryption key. This signal is intended for use to drive an external FET to illuminate an LED. This signal cannot directly drive an LED.
K1	NVMe1_TX_M	OUT	For NVMe models, this signal is the Lane 1 negative transmit signal from the module to the host.
K2	NVMe1_TX_P	OUT	For NVMe models, this signal is the Lane 1 positive transmit signal from the module to the host.
K30	IFDET_N	OUT	This is an NVMe control signal. This pin should be externally pulled low.
L29	FPGA_TDO	OUT	Reserved for future use. This pin should be left open.
M1	NVMe2_RX_M	IN	For NVMe models, this signal is the Lane 2 negative receive signal from the host to the module.
M2	NVMe2_RX_P	IN	For NVMe models, this signal is the Lane 2 positive receive signal from the host to the module.
M30	ZPM_DEVSLP	IN	This signal, when high, places the module into a deep sleep power saving mode.

Ball Descriptions (continued)

Ball No.	Ball Name	I/O	Description
N29	PS_PWR_ MEASURE	IN	Voltage input that allows the module to measure the voltage of the external main supply rail. The external main supply rail voltage must be scaled by that a 5V is presented as 1.2V to the module.
N31	TP7	OUT	Reserved for future use. This pin must be left open.
P1	NVMe2_TX_M	OUT	For NVMe models, this signal is the Lane 2 negative transmit signal from the module to the host
P2	NVMe2_TX_P	OUT	For NVMe models, this signal is the Lane 2 positive transmit signal from the module to the host
P30	TP6	OUT	Reserved for future use. This pin must be left open.
R29	TP5	OUT	Reserved for future use. This pin must be left open.
T1	NVMe3_RX_M	IN	For NVMe models, this signal is the Lane 3 negative receive signal from the host to the module.
T2	NVMe3_RX_P	IN	For NVMe models, this signal is the Lane 3 positive receive signal from the host to the module.
T31	TP4	OUT	Reserved for future use. This pin must be left open.
U30	TP3	OUT	Reserved for future use. This pin must be left open.
V1	NVMe3_TX_M	OUT	For NVMe models, this signal is the Lane 3 negative transmit signal from the module to the host.
V2	NVMe3_TX_P	OUT	For NVMe models, this signal is the Lane 3 positive transmit signal from the module to the host.
V29	TP2	OUT	Reserved for future use. This pin must be left open.
V31	TP1	OUT	Reserved for future use. This pin must be left open.
W26	OVER85C_LED	OUT	During normal operation, this signal will be low. When the module internal temperature exceeds 85C, this signal will transition from a low level to a high level. This signal is intended to drive an external FET to illuminate an LED. This signal cannot directly drive an LED.
W28	PASSWORD_LED	OUT	This signal goes high to indicate to a user that the module is waiting for entry of a password. This signal is intended to drive an external FET to illuminate an LED. This signal cannot directly drive an LED.
W30	TP0	OUT	Reserved for future use. This pin must be left open.
Y5	MON_232TX	OUT	Security port RS-232 TX output signal. This is the LV_{TTL} RS-232 transmit signal from the module to the host. This signal and the MON-232RX form a security port that allows a host to configure the module for pre-boot security features and to read status from the module.
Y7	SMDATA	IN/ OUT	Reserved for possible future use. I2C SM-Bus Data input/output from NVMe/PCIe. This signal is part of the standard NVMe signal set but it is not currently supported by the module.
Y23	REFCLK_P	IN	Positive Reference clock from the NVMe/PCIe/SATA connector.
Y25	VBAT_K81	IN	When the module is configured to utilize a battery backed up encryption key value, this pin supplies the voltage to internally hold up the AES key value. Current draw for this pin is about 10uA at 3V.
Y27	MODE_LED_GREEN	OUT	Power and normal operation LED. When the module is operating normally, this signal will be high. This signal is intended to drive an external FET to illuminate an LED. This signal cannot directly drive an LED.
AA5	MON_232RX	IN	Security port RS-232 RX input signal. This is the LV_{TTL} RS-232 receive signal from the host to the module. This signal and the MON-232TX form a security port that allows a host to configure the module for pre-boot security features and to read status from the module.
AA7	SMCLK	IN/ OUT	Reserved for possible future use. I2C SM-Bus Clock input/output from NVMe/PCIe. This signal is part of the standard NVMe signal set but it is not currently supported by the module.
AA23	REFCLK_N	IN	Negative Reference clock from the NVMe/PCIe/SATA connector.
AA26	PRSNT_N	OUT	The is an NVMe control signal. This pin should be externally pulled low.
AA28	MODE_LED_BLUE	OUT	Error mode indicator. When the module is operating normally, this signal will be low. If the module encounters an unrecoverable error, this signal will transition to a high level. This signal is intended to drive an external FET to illuminate an LED. This signal cannot directly drive an LED.

NOTE:
1. Unless otherwise specified, module input and output signals are 3.3V LV_{TTL}
2. The drive direction of all signals are with respect to the SSD module. An input is an input to the SSD module. An output is an output from the SSD module.

Ball Positions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	1
A	MISSING BALL	NC	Vss	Vss	UP_ KEYFILL_ 232TX	Vss	DN_ KEYFILL_ 232RX	Vss		Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
B	NC	Vss		Vss	UP_ KEYFILL_ 232RX	Vss	DN_ KEYFILL_ 232TX	Vss		Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
C	Vss	Vss									MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
D	NVMe0_ SATA_ RX_P	NVMe0_ SATA_ RX_M							Vss	1.2V	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
E	Vss	Vss						Vss	1.2V	Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
F	NVMe0_ SATA_ TX_P	NVMe0_ SATA_ TX_M				0.72V	Vss	0.72V	Vss	1.2V	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
G	Vss	Vss				Vss	0.72V	Vss	0.72V	Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
H	NVMe1_ RX_M	NVMe1_ RX_P				0.72V	Vss	0.72V	Vss	1.2V	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
J	Vss	Vss				Vss	0.72V	Vss	0.72V	Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
K	NVMe1_ TX_M	NVMe1_ TX_P				0.72V	Vss	0.72V	Vss	1.2V	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
L	Vss	Vss				Vss	0.72V	Vss	0.72V	Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
M	NVMe2_ RX_M	NVMe2_ RX_P				0.72V	Vss	0.72V	Vss	1.2V	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
N	Vss	Vss				Vss	0.72V	Vss	0.72V	Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
P	NVMe2_ TX_M	NVMe2_ TX_P				0.72V	Vss	0.72V	Vss	1.2V	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
R	Vss	Vss				Vss	0.72V	Vss	0.72V	Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
T	NVMe3_ RX_M	NVMe3_ RX_P				0.72V	Vss	0.72V	Vss	1.2V	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
U	Vss	Vss						Vss	1.2V	Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
V	NVMe3_ TX_M	NVMe3_ TX_P							Vss	1.2V	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
W	Vss	Vss									MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
Y	NC	Vss		Vss	MON_ 232TX	Vss	SMDATA	Vss		Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
AA	NC	NC	Vss	Vss	MON_ 232RX	Vss	SMCLK	Vss		Vss	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISS BA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	1

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss		Vss		WRITE_ PROTECT_ N		MOD_ ACTIVE	Vss	NC	NC	A
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss		Vss	PS_LOW	Vss	LINK_ SPEED_ LED_N			Vss	NC	B
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL		1.8V		3.3V		Vss	ERASE_ TRIGGER	Vss	FACTORY_ LED	Vss	C
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	1.8V	Vss	3.3V		3.3V			DESTRUCT	SHUT_ DWN_N	ACTIVITY	D
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	3.3V	Vss	3.3V	Vss		Vss	DUAL PORTEN_ N	AUTH	1.8V	E
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	1.2V	Vss	3.3V	Vss	3.3V	Vss		1.8V	Vss	BKUP_ MEASURE	F
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	3.3V	Vss	3.3V	Vss		Vss	FPGA_ TMS		1.8V	G
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	1.8V	Vss	3.3V	Vss	3.3V	Vss		1.8V	FPGA_ TCK	Vss	H
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	1.2V	Vss	3.3V	Vss		Vss	FPGA_TDI		KEY_LED	J
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	1.2V	Vss	3.3V	Vss	3.3V	Vss		1.8V	IFDET_N	Vss	K
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	1.2V	Vss	3.3V	Vss		Vss	FPGA_ TDO	Vss	1.8V	L
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	1.2V	Vss	3.3V	Vss	3.3V	Vss		1.8V	ZPM_ DEVSLP	Vss	M
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	1.2V	Vss	3.3V	Vss		Vss	PS_PWR_ MEASURE		TP7	N
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	1.8V	Vss	3.3V	Vss	3.3V	Vss		1.8V	TP6	Vss	P
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	3.3V	Vss	3.3V	Vss		Vss	TP5		1.8V	R
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	1.2V	Vss	3.3V	Vss	3.3V	Vss		1.8V	Vss	TP4	T
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	3.3V	Vss	3.3V	Vss		Vss		TP3	1.8V	U
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	1.8V	Vss	3.3V	Vss	3.3V			TP2		TP1	V
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	1.8V	Vss	3.3V	OVER85C_ LED	Vss	PASS WORD_ LED	Vss	TP0	Vss	W
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	REFCLK_P	Vss	VBAT_K81	Vss	MODE_ LED_ GREEN			Vss	NC	Y
SING ALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	MISSING BALL	Vss	REFCLK_N	Vss		PRSNT_N		MODE_ LED_BLUE	Vss	NC	NC	AA
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Part Numbering *(dashes in the part number are required)*

x BA xxx x M 6 S - 123 I xx - aa

Product Series
M = TRRUST-Stor® series, standard model without FIPS 140-2, Common Criteria or CSfC certifications

Form Factor
BA = 32mm x 22mm x 5.5mm BGA

NAND Capacity available to Host
080 = 80 GB host accessible capacity
160 = 160 GB host accessible capacity

Encryption
A = AES-256 XTS,
Q = Quantum Encryption (Planned),
N = No Encryption.

Media Manufacturer
M = Standard Product

Media Type
6 = 3-bit TLC 3D NAND

Mode
S = SLC mode.

–

Customizable Features
000 = Standard product

Operating Temperature
I = Industrial (-40 °C to +85 °C)
C = Commercial (0 °C to 70 °C)

Classification
ES = Engineering Sample
00 = Standard product

–

Attributes

- 01	Construction:	Lead Free (R)
	Interface Structure:	1 Lane (1)
	Interface Type:	SATA 6 Gb/s (SA)
- 02	Construction:	Lead Free (R)
	Interface Structure:	1 Lane (1)
	Interface Type:	NVME (NV)
- 03	Construction:	Lead Free (R)
	Interface Structure:	2 Lane (2)
	Interface Type:	NVME (NV)
- 04	Construction:	Lead Free (R)
	Interface Structure:	4 Lane (4)
	Interface Type:	NVME (NV)

Example part Number: MBA160AM6S-000IC-01

Notes

Need More Help?
Need a Variant of This Product?

Contact Mercury's Secure SSD application engineering team at secure.ssd@mrcy.com

Download our
Secure SSD Tech Brief

Download our
Demystifying Hardware
Full Disk Encryption
Technology for Military
Data Storage

Download our
Safeguarding Mission
Critical Data Whitepaper

Download our
Microelectronics
Quick Reference Guide

5023.05E-0418 ds SSD Mercury TRRUST-Stor BGA SSD

mercury systems™
INNOVATION THAT MATTERS™

Corporate Headquarters
50 Minuteman Road
Andover, MA 01810-1008 USA
+1 (978) 967-1401
+1 (866) 627-6951
Fax +1 (978) 256-3599

Microelectronic Secure Solutions
3601 East University Drive
Phoenix, AZ 85034-7217 USA
+1 (602) 437-1520
Fax +1 (602) 437-1731

MADE IN AMERICA